UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/871,084	05/30/2001	Frederick D. Weber	TT3763	2031

23720 7590 05/10/2005

WILLIAMS, MORGAN & AMERSON, P.C.
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

EXAMINER	
ZAND, KAMBIZ	

ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/871,084	WEBER ET AL.	
	Examiner	Art Unit	
	Kambiz Zand	2132	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) *1-29 and 58-62* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *30-57 and 63-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/03/2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Election of Group invention III, claims 30-57 and 63-70 with traverse have been acknowledged.
2. Claims 1-29 and 58-62 have been withdrawn from examination.
3. **Claims 30-57 and 63-70** have been examined.
4. All co-pending applications relating to the present application have been considered.
5. Priority benefit claimed under Title 35, United States Code, § 120 have been acknowledged.

Information Disclosure Statement PTO-1449

6. The Information Disclosure Statement submitted by applicant on 10/03/2002 has been considered. Please see attached PTO-1449.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

8. **Claims 45, 46, 55 and 68** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- **In claim 45**, the "substantially" phrases makes the claims indefinite and unclear in that neither means nor interrelationship of means are set forth in these claims in order to achieve the desired results expressed in the "substantially" phrases. The phrase is relative term. Examiner suggests deletions of relative terms from claim language. Corrections is requested.

- **In claim 46, 55 and 68** the "in lieu of data" phrases makes the claims indefinite and unclear in that neither means nor interrelationship of means are set forth in these claims in order to achieve the desired results expressed in the "in lieu data" phrases. The phrase is a confusing term since any response contains data. Corrections or clarification is requested. If Applicant traversing the rejection, then the clarification should be specific to which embodiment of the invention such phrase is related and where in the specification it has such support.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude"

granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims **30, 50 and 63** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 21; and 40, of Co-pending application number 09/852,372. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Claim(s) 21 and 40 of Co-pending application number 09/852,372 contain(s) every element of claim(s) 50 and 63 of the instant application **respectively** and as such anticipate(s) claim(s) 50 and 63 of the instant application.

Claim(s) 1 of Co-pending application number 09/852,372 contain(s) every element of claim(s) 30 of the instant application **respectively,** excluding the limitation "wherein the security hardware includes a lock override register configured to deny access to the secure assets when a lock override bit is set". Claim(s) 30 of instant application have the added feature "wherein the security

hardware includes a lock override register configured to deny access to the secure assets when a lock override bit is set", however the instant claim 30 is obvious from claims 1 of copending Application No. 09/852,372 since the implementation of the method of copending Application No. 09/852,372 requires having "a lock override register configured to deny access to the secure assets when a lock override bit is set" and therefore it would have been obvious to include "a lock override register configured to deny access to the secure assets when a lock override bit is set" in order to implement the claimed method in case of digital signature verification failure.

A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. **Claims 30, 45, 50 and 63** are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi et al. (U.S. Patent No. 56152633).

As per claim 30, 50 and 63 Takahashi et al. teach "A secure mode within a dual mode processor
is implemented" (Abstract) reads on claim 30 wherein a processor is configured to operate in an operating mode, wherein the operating mode is one of a plurality of operating modes including a secure operating mode.
Takahashi et al. teach primitives which encrypt/decrypt the data (secure assets), 1/0 hardware control circuit and assurance logic (security hardware) (col.2 lines 10-13, col. 3 lines 53-59 and col. 4 lines 29-34) which read on "security hardware configured to control access to the secured assets dependant upon the operating mode of the processor, wherein the security hardware is configured to allow access to the secure assets in the secure operating mode".

As per claim 45 Takahashi et al. teach that in while in secure mode, processing functions execute only the secure primitives in ROM but they still have the ability to access external memory for data (col.3 lines 53-57), which reads on the processor being configured to store and retrieve data from the memory in all of the plurality of operating modes.

2. **claims 30, 32-38, 48, 50 and 63** are rejected under 35 U.S.C. 102(e) as being anticipated by Angelo et al. (U.S. Patent No. 6581 162).

As per claim 30, 50 and 63 Angelo et al. teach method for securely managing

encryption
information in a computer system, having a secure mode of operation and a normal mode of operation" (col 10 lines. 53-55) which read on the limitation "a processor configured to operate in an operating mode, wherein the operating mode is one of a plurality of operating modes including a secure operating mode".
The limitation "one or more secured assets coupled to the processor" is met by secure memory (col. 3 lines 12-16).
Furthermore, Angelo et al. teach storing an encryption algorithm in a secure memory space not accessible to the normal software processes and only accessible by the general processor in the secure mode of operation" (col 10 line 66- col. 11 line 2) and PCI-ISA bridge to allow access to protected resources (col. 4 lines 56-649. This reads on security hardware configured to control access to the secured assets dependant upon the operating mode of the processor, wherein the security hardware is configured to allow access to the secure assets in the secure operating mode"

As per claim 32-33 Angelo et al. teach system management mode (SMM) which is entered upon receipt of a system management interrupt (SMY). Angelo ef al. also teach SMI asserted by either an SMI timer or by a system request upon which the entire CPI state is saved in the SMM memory. After the initial processor state is saved, the processor begins executing an SMI handler routine providing security services (col 7 line 43- col. 8 line 43.
The above reads on receiving a request to change the computer system from the first operating mode to the secure operating mode, providing an entry into an initiation register and accessing the control signal indicative of the entry providing a system management interrupt.

As per claims 34-38 Angelo et al. teach timers (col. 4 line 58). When the computer system detects a request for secure communications or any event

requiring secure entry of encryption information. Control then proceeds to step where appropriate registers in processor are loaded prior to execution of the SMI code (Fig. 5, col. 9 lines 3-13). The computer systems don't wait indefinitely for input of the sensitive information like passwords. Timer measuring a time period in which the computer system is in the secure operating mode, and providing a control signal to exit the secure mode in response to the time period in which the computer system is in the secure operating mode exceeding a predetermined length of time are used complete indefinite sessions.

As per claim 48 Angelo et al. teach a battery providing reserve power to the security hardware (col. 8 lines 23-25).

3. **Claims 30, 50 and 63** are rejected under 35 U.S.C. 102(b) as being anticipated by Angelo et al. (U.S. Patent No. 57488883).

As per claim 21, 50 and 63 Angelo et al. teach a method for providing access to secured assets in a computer system, the method including switching the computer system between a first operating mode and a second operating mode where the second operating mode includes a secure operating mode (col. 2 lfnes 40-51 and Fig. 2 steps 404-4103. The access to the secured assets is permitted in response to the computer system being in the secure operating mode and restricted when in the first operating mode.

4. **Claims 30, 44, 50 and 63** are rejected under 35 U.S.C. 102(b) as being anticipated by Hadfield et al. (Lee Hadfield, Dave Hatter, Dave Bixler, "Windows NT Server 4 security handbook",1997, ISBN.. 078971213-x.).

As per claims 30, 44, 46, 50, 55, 63 and 68 Hadseld et al. teach that a processor is configured to operate in an

operating mode, wherein the operating mode is one of a plurality of operating modes including a secure operating mode and secure apsets (e.g. files) that can only be accessed in the secure mode. Windows NT runs on hardware, the computers which use processors. Each user that accesses any Windows NT Server-based resources first must be validated by the system, and the user is required to enter a valid password before any interactive Windows session is allowed (pg. 45, UserAccounts in a Windows NT Environment).

As per claim 44 the limitation "scratchpad RAM, wherein each of the one or more Page 8 secured assets is configured to access the scratchpad RAM for the storage of data" computers store applications and files accessed by users in (scratchpad) RAM.

As per claims 46, 55 and 68 computer RAM in Windows NT Server stores input and output data in memory banks (mailbox RAM), and the input data for the one or more secured assets is addressed to the RAM and the output data is retrieved from an address at the RAM. Also, as discussed above in reference to claim 1, users don't have access to the system until the log-on sequence allows them to log-on to the system and enter the secure mode. It is inherent to have filters configured not to provide input data to RAM if the processor is not operating in the secure operating mode.
Upon receipt of the access request if the processor is not operating in the secure operating mode (placing an incorrect password and/or user name while attempting to access the system) will result in an error message and denial of access to the system will result in a predetermined response in lieu of data.

All other claims limitations excluding the allowable subject matters below are taught by the above references either single or in combination. Please see the entire references.

Allowable Subject Matter

10. Claims 40-43, 54, 56, 67 and 69 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. Please see enclosed pto-892.
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kambiz Zand whose telephone number is (571) 272-3811. The examiner can normally reached on Monday-Thursday (8:00-5:00). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gilberto Barron can be reached on (571) 272-3799. The fax phone numbers for the organization where this application or proceeding is assigned as (703) 872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kambiz Zand

05/05/2005